



The Chinese University of Hong Kong
Non-confidential Abstract of Technology Disclosure

Title:

Improving FPGA Technology Mapping and Routing, and Sequential Circuit Retiming by Logic Rewiring Operations

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Patent Status: US Patent Pending

Non-confidential abstract:

In this application, we propose strategies for using a so-called Rewiring technique for the following VLSI Electronic Design Automation (EDA or CAD) operations: FPGA Technology Mapping and Routing, and Sequential Circuit Retiming.

Rewiring is a logic perturbation technique that replaces a signal wire/gate with other wires/gates without changing the logic function of a circuit. It appeals like some new signal wire/gate is added to replace some old signal wire/gate, which can be served as a circuit transformation process. In today's VLSI chips, because of the continual scaling down on transistor sizes, the wiring delay has become a much dominating factor than gate delay and often becomes a chip's performance bottle neck. Due to its unique capability of applying logic transformation upon spotted or targeted wires, a wire-targeting capability, the Rewiring logic transformation technique can gain much higher timing accuracy and control than the old gate-based circuit transformation techniques.

One unique property of an FPGA chip is that any logic perturbation inside its Look-Up-Tables (LUTs) is totally area/delay-free. Here we propose to apply the following rewiring strategies (among others) for the optimization of FPGA Technology Mapping and Routing: (1) Replacing LUT-external wires by (resource free) LUT-internal wires, (2) Replacing longer external wires by shorter external wires, (3) Replacing wires in routing crowded area by wires in less crowded area, (4) Replacing delay-critical wires by none delay-critical wires, (5) Replacing wires with larger area-flow by wires with smaller area-flow, etc.

For the Sequential Circuit Retiming, we propose the following rewiring strategies: (1) Record flip-flop positions after retiming and replace wires connected to flip-flop by alternative wires at non-flip-flop location, (2) Replace wires with smaller slack by wires with larger slack for delay optimization. (3) Replace wires by alternative wires with less flip-flop overhead upon retiming.

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