



The Chinese University of Hong Kong
Non-confidential Abstract of Technology Disclosure

Title:

Enhancing FPGA Technology mapping by Logic Rewiring

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Patent Status:

US Patent Pending

Inventor(s):

Professor Yu Liang David WU, Department of Computer Science and Engineering

Non-confidential abstract:

Field Programmable Gate Array (FPGA) is a device with pre-fabricated, programmable interconnects and logic blocks. The performance of the circuit heavily depends on the efficiency and the optimization power of the design automation system. Technology mapping is one of the most crucial stage of FPGA design flow: a good mapping with smaller depths and areas will significantly improve chip utilization and circuit speed. As over 80% of delay comes from interconnect delay under today's deep micron circuit, traditional gate-conscious logic synthesis system can no longer well optimized the circuit for delay performance and will be outweighed by the innovative, wire-conscious approach in this invention.

We propose a logic-aware and generic method which can further reduce both depth and area for the FPGA mapped results produced by other excellent tools. This invented technique has been tested with various state-of-the-art FPGA technology mapping tools in both academia and industry and has demonstrated its universal capability of improving further upon all these tools. Our extensive experiments show that our method is promising and effective: a combination of logic level reduction and area minimization techniques can improve both the LUT depth and area by 11.% (vs. FlowMap) and 6.1% (vs. FlowSYN) respectively. The area improvements are up to 33.7% (avg. 11.4%) vs DAOMap. The proposed method combines logic perturbation and technology mapping algorithms for further area/depth reduction. Our results fully demonstrate that our wire-conscious based logic perturbation scheme can always explore a new optimization domain the current other technology mapping techniques can not explore and brings better FPGA technology mapping results.

For further queries, please contact:

Mr Billy Lam
Technology Licensing Coordinator
Tel: (852) 2609 8882
Fax: (852) 2603 5451
Email: billylam@cuhk.edu.hk

Address:
Technology Licensing Office
The Chinese University of Hong Kong
Room 226, Pi Ch'iu Bldg, Shatin, New Territories
Hong Kong SAR