



**The Chinese University of Hong Kong**  
**Non-confidential Abstract of Technology Disclosure**

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**Title:**

**Logic Rewiring Integrated Retiming Scheme for Flip-flop Reductions**

**CUHK Ref. No.:**

08/ENG/291

**Patent Status:**

US Patent Pending

**Inventor(s):**

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**Non-confidential abstract:**

Without a mechanism to properly reflect real physical design information, the clock period produced by any retiming scheme is unrealistic and unrealizable due to the higher dominance of interconnect delays. Nonetheless, because of the difference between the fan-in and fan-out counts of a component with flip-flops retimed, in a conventional retiming procedure, the number of flip-flops could be largely increased, which can bring an undesired area penalty on the retimed circuit. To overcome these two major drawbacks of the conventional retiming technique, we propose a novel retiming flow being able to largely cut down flip-flops while with the original retimed clock period uncompromised. An effective rewiring-based optimization scheme is developed to cut down the number of flip-flops for a retiming scheme with interconnect delay formulated together and guided by placement-based delay estimations.

Experimental results show that, without compromise on the clock period reduction, this new rewiring-integrated retiming scheme can bring a large reduction of 19.1% (in average) on the number of flip-flops compared to the original retiming without rewiring.

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